REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-20 in the application. In a previous response and preliminary amendment, the Applicants amended Claims 1, 6, 8, 13-14 and 19. In the present response, the Applicants have not amended, canceled or added any claims. Accordingly, Claims 1-20 are currently pending in the application.

I. Rejection of Claims 1-20 under 35 U.S.C. §102

The Examiner has rejected Claims 1-20 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,815,016 to Erickson. The Applicants respectfully disagree.

Erickson relates to clock distribution in digital circuits and, more specifically, to a controlled delay path for phase synchronizing an output clock signal to a reference clock signal. (*See* column 1, lines 12-15.) Erickson discloses a phase-locked loop having a series of selectable voltage controlled delay elements (18, 19, 20) that can be inserted into a delay path at the choice of a user. (*See* column 4, lines 40-45 and Figure 1.) The voltage controlled delay elements are connected to a series of corresponding multiplexers (21, 22, 23) that are operated by control signals applied by a corresponding control element (24, 25, 26) to select or deselect a specific delay element or a combination of delay elements. Therefore, the delays may be introduced singly or they may be cascaded. (*See* column 5, lines 4-12 and Figure 1.)

Erickson does not disclose delivering a single signal to activate one tap to insert a corresponding delay into a PLL, wherein the corresponding delay is capable of including fixed delays associated with multiple of a plurality of taps as recited in independent Claims 1, 8 and 14. Instead, Erickson discloses inserting each individual delay element into the delay path by a separate,

corresponding control element. (*See* column 5, lines 4-12; column 7, lines 26-39; and Figure 1.) For example, delay element 20 is inserted into the delay path by control element 26 and delay element 19 is inserted by control element 25. Similarly, a single signal is not capable of including multiple multiplexers in the delay path. (*See* Figure 1.) Accordingly, Erickson discloses employing multiple signals to insert multiple delays into the delay path. As such, Erickson fails to teach delivering a single signal to insert a corresponding delay capable of including fixed delays associated with multiple of a plurality of taps as recited in independent Claims 1, 8 and 14.

Therefore, Erickson does not disclose each and every element of independent Claim 1, 8 and 14 and Claims dependent thereon. As such, Erickson does not anticipate independent Claims 1-20. The Applicants, therefore, respectfully request the Examiner to withdraw the §102 rejection with respect to Claims 1-20 and allow issuance thereof.

II. Comment on Cited References

The Applicants reserve further review of the references cited but not relied upon if relied upon in the future.

III. Conclusion

In view of the foregoing remarks, the Applicants see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-20.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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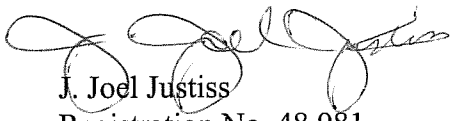

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